LIQUID CRYSTAL DISPLAY DEVICE FOR DISPLAYING VIDEO DATA

BACKGROUND OF THE INVENTION

Field of the Invention

This invention concerns a display device for displaying video data (including image data and text data) and more in particular it relates, for example, to a liquid display device, CRT (Cathode Ray Tube) display device, plasma display device or EL (Electroluminescence) display device.

Description of Related Art

Existent color conversion methods for video data from video signal generation devices and conversion devices therefor have been adapted, as disclosed, for example, in J-P-A No. 11-275375, to set correction values to lattice point data for strengthening positions in a possible range of color values after conversion to a poly-dimension lookup table so as to allow values out of the possible range for the color values after conversion, to thereby conduct desired color conversion as much as possible, input color signals for color conversion to an address generation section upon color conversion and conduct interpolation by an interpolation operation section based on lattice point

data outputted from the poly-dimension lookup table to obtain color values after conversion corresponding to the inputted color signals and, when the color values after conversion are out of the possible range, convert them to boundary values by a gradation conversion section.

However, although the prior art described above discloses a basic concept of setting lattice point color values for the boundary portions of the possible range for the color values after conversion to the poly-dimension lookup table and conducting operation for the portion between lattice points thereby enabling color conversion without increasing the capacity of the lookup table, it does not mention to a lookup table setting means for analyzing input video data to conduct optimal display corresponding to the condition of the input video data.

Further, although the prior art discloses above describes the color conversion method by the video data by the setting of the lookup table and the operation method for the lattice points by the set value, it does not describes means for obtaining a satisfactory display, for example, state by combining back light control.

As another prior art, there has been known to expand a bright gradation or dark gradation by a γ-correction circuit corresponding to high or low level of APL (Average Picture Level) of video signals to improve the contrast of

display images in a liquid crystal display device. For example, a γ-correction circuit described in J-P-A No. 6-6820 has a γ-correction memory that stores γ-correction data for white level expansion and γ-correction memory that stores γ-correction data for black level expansion and selects one of the γ-correction memories depending on whether the APL of the video signals is higher or lower than a predetermined value, to conduct γ-correction for the video signal. This can expand for the bright gradation or dark gradation in accordance with high or low level of APL in the video signal and can improve the contrast of the displayed images in the liquid crystal display device.

Video signals displayed on the liquid crystal display devices includes video images of television broadcasting, as well as video signals regenerated from VTR or DVD, video images photographed by video cameras and video images prepared by computer graphics. Further, since the number of broadcasting channels has been increased greatly by transfer from existent analog broadcasting to digital broadcasting such as satellite broadcasting, and video signal sources have become more and more versatile. Further, such versatile video signals have been introduced also in computers in addition to existent television broadcasting, where they are displayed as display data of

computers and, further, such video signals will be processed and fabricated and displayed on display devices.

In a case of displaying such versatile video signals on liquid crystal display devices, various kinds of γ-correction memories have to be provided corresponding to gradation characteristics for all sorts of video signals in the prior art which is adapted to select one of plural γ-correction memories previously provided in accordance with high or low APL in the video signals to conduct γ-correction for the image signals. Further, video image scenes actually change sequentially and currently with time for video signals, but provision of a number of γ-correction memories optimal to each of the video image scenes requires a great amount of memories to result in increase of the cost and is not practical. Further, in the selection of the γ-correction memory in accordance with APL in the video signals, one identical γ-correction memory is selected for different video image scenes so long as the APL is identical. However, in a case of low APL, for instance, this means that an identical γ-correction is applied irrespective that the entire screen shows a dark video image scene in average, or a video image scene in which a bright area is locally present in entirely dark area. While γ-correction should be different between such cases, the γ-memory is selected in accordance with APL in the video signals in the prior art,

so that fine γ-correction depending on the video image scenes can not be conducted.

Furthermore, in CRTs used generally so far as display devices, electric signal and brightness are in a $n^{2.2}$ but the liquid crystal display device has a characteristic that the relation between the amount of light transmitting the liquid crystal and the electric signal is saturated both in a dark area and a bright area as shown in Fig. 25. Then, it is necessary to conduct γ-correction for video signal while taking such characteristic inherent to the liquid crystal display device into consideration.

SUMMARY OF THE INVENTION

This invention intends to provide an appropriate contrast in accordance with video data and provide a liquid crystal display device capable of clearly displaying video images.

Further, this invention intends to provide a liquid crystal display device capable of clearly displaying video images by obtaining an appropriate light amount of a back light in accordance with video data.

Further, this invention intends to provide a liquid crystal display device capable of improving the efficiency of utilizing the light of a back light or capable of reducing

the electric consumption power for lighting up the back light by obtaining an appropriate amount of light of the back light in accordance with the video data.

In this invention, a luminance characteristic relative to the gradation of inputted video data is detected, the gradation is corrected in accordance with the luminance characteristic and the corrected gradation is displayed on a liquid crystal panel.

Preferably, the gradation is corrected such that the luminance of a gradation of higher generation frequency than other gradation is relatively higher compared with that of other gradation.

Preferably, gradation is corrected so as to emphasize black color when a gradation of higher generation frequency is situated on the side of a gradation of relatively lower level in the luminance characteristic.

Preferably, gradation is corrected so as to emphasize white color when a gradation of higher generation frequency is situated on the side of a gradation of relatively higher level in the luminance characteristic.

Preferably, gradation is corrected such that the luminance of a gradation containing a maximum luminance value in the luminance characteristic approaches a maximum luminance value that the liquid crystal panel can display.

Preferably, gradation is corrected such that the luminance of a gradation containing a minimum luminance value in the luminance characteristic approaches a minimum luminance value that the liquid crystal panel can display.

Further, in this invention, a luminance characteristic relative to the gradation of inputted video data is detected and the amount of light of a back light is controlled in accordance with the luminance characteristic.

Preferably, when luminance in one or plural frames is lower compared with the luminance in other one or plural frames, the amount of light of a back light is decreased relatively.

Preferably, when luminance in one or plural frames is higher compared with the luminance in other one or plural frames, the amount of light of the back light is increased relatively.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-described and other objects, advantages and novel features of this invention will become more apparent from the following description in this specification when taken in conjunction with the accompanying drawings, wherein

Fig. 1 is a schematic view for a system constitution of a display device as a first embodiment according to this invention;

Fig. 2 is a detailed view for a system constitution of a display device as a first embodiment according to this invention;

Fig. 3 is a detailed view for a system constitution of a luminance signal generation section in a first embodiment according to this invention;

Fig. 4 is a detailed view for a system constitution of an input video image characteristic detection section in a first embodiment according to this invention;

Fig. 5 is a detailed view for a system constitution of a polygonal line point generation section in a first embodiment according to this invention;

Fig. 6 is an input/output luminance characteristic graph in a polygonal line point generation section in a first embodiment according to this invention (first example of characteristic);

Fig. 7 is a detailed view for a system constitution of an input image characteristic feedback control section in a first embodiment according to this invention;

Fig. 8 is an input/output luminance characteristic graph in a polygonal point generation section in a first

embodiment according to this invention (second characteristic example);

Fig. 9 is an input/output luminance characteristic graph in a polygonal point generation section in a first embodiment according to this invention (third second characteristic example);

Fig. 10 is an input/output luminance characteristic graph in a polygonal point generation section in a first embodiment according to this invention (fourth characteristic example);

Fig. 11 is an input/output luminance characteristic graph in a polygonal point generation section in a first embodiment according to this invention (fifth characteristic example);

Fig. 12 is an input/output luminance characteristic graph in a polygonal point generation section in a first embodiment according to this invention (sixth characteristic example);

Fig. 13 is a detailed view for a system constitution of an inter-point gradation operation section in a first embodiment according to this invention;

Fig. 14 is a conceptional view for explaining the operation of the inter-point gradation operation section in a first embodiment according to this invention;

Fig. 15 is a detailed view for a system constitution of a display device in a second embodiment according to this invention;

Fig. 16 is a conceptional view for explaining the control of amount of light for a back light in a second embodiment according to this invention;

Fig. 17 is a flow chart for the control of amount of light for a back light in a second embodiment according to this invention;

Fig. 18 is a block diagram of a liquid crystal display device in a third embodiment according to this invention;

Fig. 19 is a constitutional view of a histogram detection circuit in a third embodiment according to this invention;

Fig. 20 is a constitutional view of a Y-value calculation circuit in a third embodiment according to this invention;

Fig. 21 is a constitutional view of a gradation control point calculation circuit in a third embodiment according to this invention;

Fig. 22 is a constitutional view of an arbitrary curve γ-correction circuit in a third embodiment according to this invention;

Fig. 23 is a graph for a histogram value outputted from a histogram detection circuit in a third embodiment according to this invention;

Fig. 24 is a graph illustrating a relation between an input gradation and an output gradation of an arbitrary curve γ-correction circuit in a third embodiment according to this invention;

Fig. 25 is a graph illustrating a relation between the amount of light transmitting a liquid crystal and an electric signal (voltage effective value) of a liquid crystal display device in a third embodiment according to this invention;

Fig. 26 is a graph illustrating a relation between input display data (gradation data) and a transmission ratio of light of a liquid crystal display device in a third embodiment according to this invention;

Fig. 27A and Fig. 27B are graphs illustrating the state of changing sections in each of histogram distribution relative to a relation between the input (gradation data) and the transmission ratio of light of liquid crystal of a liquid crystal display device in a third embodiment according to this invention;

Fig. 28 is a detailed constitutional view of a pulse generation circuit in a fourth embodiment according to this invention;

Fig. 29 is a block diagram of a liquid crystal display device in a fifth embodiment according to this invention;

Fig. 30 is a detailed constitutional view of a low-pass filter in a fifth embodiment according to this invention;

Fig. 31 is a block diagram of a liquid crystal display device in a sixth embodiment according to this invention;

Fig. 32 is a block diagram of a liquid crystal display device in a seventh embodiment according to this invention; and

Fig. 33 is a block diagram of a liquid crystal display device in an eighth embodiment according to this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of this invention is to be explained with reference to the drawings.

Fig. 1 is a constitutional view illustrating a first embodiment of a display system using the technique according to this invention.

In Fig. 1, are shown a video image characteristic detection section 1 for measuring the luminance characteristic of video signals such as luminance distribution, maximum luminance, minimum luminance and average luminance of RGB video signals, a polygonal point

generation section 2 for calculating a correction control point for gradation correction from the luminance characteristic of the video signals detected by the input video image characteristic detection section 1, a polygonal line approximation gradation correction section 3 for correcting the luminance characteristic of RGB video signals by the gradation correction control point generated by the polygonal point generation section 2 and a liquid crystal display panel 4 for displaying RGB video signals corrected with the gradation characteristic.

This invention is adapted to determine the luminance characteristic of video signals such as luminance distribution, maximum luminance or minimum luminance and average luminance on every 1 frame of the video signals inputted from television broad casting, personal computer, video tape recorder (VTR) and DVD, thereby determining the gradation characteristic on every 1 frame, conduct gradation correction to the video signals based on the determined gradation characteristic and display the same on a liquid crystal display device, to thereby improve the conspicuous or clear impression of the displayed image quality. Detailed constitution and operation of the first embodiment according to this invention are to be explained with reference Fig. 2 through Fig. 14.

In Fig. 2, are shown a switching circuit 5 for switching RGB analog video signals from a personal computer (hereinafter referred to as PC) and composite signals from a video tape recorder converted into RGB signals, an A/D converter for converting RGB analog output from the switching circuit 5 into digital data, a luminance/color signal separation control section 7 for separating the composite signals from the video tape recorder or the like into luminance signal and color signals, a signal processing control section 8 for converting the luminance signals and color signals from the separation control section 7 into RGB signal, a luminance signal generation section 9 for generating digital luminance data from the digital RGB signals from the A/D converter 6, switching circuits 10 - 12 for switching the RGB output from the A/D converter 6 and the luminance signal output (Y) from the luminance signal generation section 9, input video data characteristic detection sections (hereinafter referred to as "input video image characteristic detection section") 13 - 10 for detecting the characteristic of the input video signals in an arbitrary period from the output from the switching circuits, polygonal point generation sections 16 - 18 for generating output gradation data of each of region boundaries upon dividing the inputted entire gradation region into arbitrary regions, inter-point gradation

operation sections 19 - 21 for determining the gradation characteristic between the polygonal line points of adjacent gradation regions, a sync signal control section 22 for synchronizing horizontal, vertical and blanking period signals in the input signals from PC or composite with the output timing, a microcomputer 23 for the entire control of this control device and a display panel 4 using liquid crystal or the like as an example of a display medium, and a liquid crystal module (display device) 25 including the luminance signal generation section 9, the switching circuits 10 - 12, the input video image characteristic detection sections 13 - 15, the polygonal point generation sections 16 - 18, the inter-point gradation operation sections 19 - 21, the sync signal control section 22 and the display panel 4. Since the polygonal point generation sections 16 - 18 convert the gradation characteristic of the input video signal in accordance with the input video signals, it can be said that the circuits operate as the gradation correction coefficient generation sections that generate correction coefficient for correcting the input video signals based thereon. The inter-point gradation operation sections 19 - 21 output data corrected by the correction coefficient generated from the gradation correction coefficient generation section to the input video signals.

The entire operation of the first embodiment according to this invention is to be described with reference to Fig. 2.

At first, the switching circuit selects signals of RGB analog video image input such as from PC or composite video image input such as from a video tape recorder converted into RGB analog signals. For converting the composite video image input into the RGB analog video signals, they are at first separated into luminance signals and color signals in the luminance/color signal separation processing section 7 and then the signals are processed into color difference signals by the signal processing control section 8 and then converted into RGB analog signals and outputted. RGB analog video signals selected by the switching circuit 5 are converted by the A/D converter 6 into digital signals and then inputted to the switching circuits 10 - 12 and also to the luminance signal generation section 9. The luminance signal generation section determines a luminance value (Y) on every picture element (the picture element is data for R, G and B together) from the inputted RGB digital video data and outputs the results to the switching circuit 10 - 12. The switching circuits 10 - 12 select either the RGB video data from the A/D converter 6 or the luminance data (Y) from the luminance signal generation section 9 and outputs the same to the input video image characteristic detection

sections. The input video image characteristic detection sections 13 - 15 are circuits for detecting the luminance characteristic of the video signal appearing in 1 frame such as luminance distribution expressing the ratio for each luminance, max · min luminance and average luminance on every one frame from the RGB video data or the luminance data (Y). Then, upon detection from the RGB video data, the characteristic on every colors can be detected by providing 3 systems of identical circuits for each of color and, on the other hand, upon detection of the luminance characteristic from the luminance data (Y) from the luminance signal generation circuit 9, the characteristic on every picture elements can be determined by 1 system of circuits. The input video image characteristic detection sections 13 - 15 detect the gradation distribution characteristic, gradation maximum value · minimum value and the gradation mean value from the inputted RGB video data or luminance data (Y) inputted on every 1 frame and output them to the microcomputer control section 24. In a case where the video data change frequently such as in dynamic images from a video tape recorder, the luminance characteristic of the video signals is detected on every 1 frame and in a case where the motion is relatively small as in the video images from PC, the luminance characteristic

of the video signals can be detected for plural frames as one period.

Then, detected data showing the luminance characteristic of the video signals detected in the input video image characteristic detection sections 13 - 15 are sent to the microcomputer control section 23. The microcomputer control section 24 outputs the detected data from the input video image characteristic detection sections 13 - 15 to the microcomputer 23 in accordance with the demand from the microcomputer 23. The microcomputer 23 generates polygonal line point data based on the detected data and outputs them to the microcomputer control section 24. The method of generating the polygonal line point data will be detailed later. The microcomputer control section 24 outputs the polygonal line point data to polygonal point generation sections 16 - 18. The polygonal point generation sections 16 - 19 output polygonal line point data from the microcomputer control section 24 to the inter-point gradation operation sections 19 - 21. The inter-point gradation operation sections 19 - 21 convert the gradation characteristic of the RGB digital video data from the A/C converter 6 in accordance with the polygonal line point data and output the gradation data after conversion to the display panel 4. Since the digital video data from the A/D converter 6 are different for R, G and B in each case of the

detection modes for the input video data characteristic, that is, in a case of detection for each of R, G and B colors and in a case of detection for the luminance data (Y) from the luminance signal generation section 9, each of the inter-point gradation operation sections 19 - 21 comprises three systems of circuits.

Details for the functions in each of the sections are to be explained.

Fig. 3 is an explanatory view for the operation of the luminance signal generation section 9 in a first embodiment. The ratio between each of the colors in a case of generating the luminance data (Y) from the RGB video data is expressed, for example, by the following equation:

$$\text{Luminance Data } (Y) = 0.299 \times R(\text{red}) + 0.587 \times G(\text{green}) + 0.144 \times B(\text{blue})$$

The equation for calculating the luminance data (Y) is an operation for the sum of products of the RGB video data each appended with a real number coefficient, and it is difficult to process the same exactly by hardware in view of increase in the scale of the circuits and lowering of the processing speed. Then, the operation is simplified for easy attainment of the operation for the sum of products by the hardware. Since the generated luminance data per se are not the display data but for obtaining the characteristic of the display data, this is attained by bit shifting and

addition processing. In Fig. 3, the following approximation processing to the equation described above is enabled assuming each of R, G and B as 8 bit digital video data, and by rightward shifting for the R color each by 2 bits and 5 bits (rightward shifting by one bit for division by 2, rightward shifting by n bits for division by 2^2), rightward shifting for the G color each by one bit and 4 bits, and rightward shifting for B color by 3 bits and by adding all of the shift data.

$$\text{Luminance Data (Y)} = 0.281 \times \text{R(red)} + 0.563 \times \text{G(green)} + 0.125 \times \text{B(blue)}$$

Since the operation processing for generating the luminance data (Y) can be simplified as described above, simplification can be attained easily by the hardware. Alternatively, it may be attained also by software.

Then, detailed constitution and operation of the input video image characteristic detection sections 13 - 15 in Fig. 2 are to be explained with reference to Fig. 4.

In Fig. 4, are shown a detection setting section 26 for setting the detection period for once, an input gradation divisional number setting section 27 for setting a divisional number in the entire input gradation region, an input image data gradation region detection section 28 for detecting the correspondence of the input video data to each of the divisional region set by the input gradation

divisional number setting section 27, a first gradation region counter 29 for counting the data in the region of the lowest gradation, a second gradation region counter 30 for counting the data in the region of the gradation next to the lowest, an n_{th} gradation region counter 31 for counting the data in the region of the highest gradation, a first distribution data hold latch 32 for holding the total number of data in the region for the lowest gradation in the detection period for once, a second distribution data hold latch 33 also for holding the total number of data in the second region, an n_{th} distribution data hold latch 34 for holding the total number of data in the region for the highest gradation, an n multiplier circuit 35 for multiplying the counted value of the first gradation region counter 29 by the factor of m, a 2*m multiplier circuit 36 for multiplying the counted value of the second gradation region counter 30 by the factor of 2*m, an n*m multiplier circuit 37 for multiplying the counted value of the n_{th} gradation region counter 31 by the factor of n*m, an adder circuit 38 for adding output data from each of the multiplier circuits, an n*m divider circuit 39 for dividing the output from the adder circuit 38 by the factor of n*m, an average luminance data hold latch 40 for holding the output from the divider circuit 39 as an average luminance value, a comparison circuit 41 for comparing the video data under

serial sending with the output of a dot data latch circuit 43 to be described later and selecting and outputting larger data, a comparison circuit 42 for comparing the video data under serial sending with the output of a dot data latch circuit 43 to be described later and selecting and outputting smaller data, a dot data latch circuit 43 for latching the output from the comparison circuit 41, a dot data latch circuit 44 for latching the output of the comparison circuit 42, a maximum luminance data hold latch 45 for holding the maximum luminance data as the output data from the dot data latch circuit 43 in an arbitrary period set by the detection setting section 26, and a minimum luminance data hold latch 46 also for holding the minimum luminance data as the output data from the dot data latch circuit 44 in the arbitrary period set by the detection setting section 26.

Further, a luminance distribution detection section 200 for detecting the luminance distribution of the input image data comprises the input video data gradation region detection section 28, the first gradation region counter 29, the second gradation region counter 30, the n_{th} gradation region counter 31, the first distribution data hold latch circuit 32, the second distribution data hold latch 33 and the n_{th} distribution data hold latch 34. A luminance average value detection section 201 for detecting the average

luminance of the input video data comprises the m multiplier circuit 25, 2*m multiplier circuit 36, the n*m multiplier circuit 37, the adder circuit 38, the n*m divider circuit 39 and the average luminance data hold latch 40. A luminance max · min value detection circuit 202 for detecting the maximum value and/or minimum value for the luminance of the input video data comprises the comparison circuits 41, 42, the dot data latch circuits 43, 44, the maximum luminance data hold latch 45 and the minimum luminance data hold latch 46.

At first, the detection period for once is set to the detection setting section 26 under the control of the microcomputer control section 24. In this embodiment, since the contents of the display change on every frame as in the video signals, explanation is to be made for the case where the detection period for once is set as one frame. In a case where the contents of display change scarcely as in the personal computer, the detection period for once may be set as plural frames. The output from the detection setting section 26 forms a latch clock for the final stage data hold latch in each of the detection function sections as will be described later. On the other hand, the number for dividing the magnitude of the brightness of the input image data (for example, luminance data (Y)) is set by the input gradation divisional number setting section 27 under the control of

the microcomputer control section 24. As an example, the entire input region is defined as 256 gradations (8 bit) and the divisional number is set as 8 for division. The output from the input gradation divisional number setting section 27 is inputted to the input video data gradation region detection section 28, which judges the correspondence of the gradation value of the input video data to each of the divisional regions from the input gradation divisional number setting section 27 and outputs a clock for the region counter corresponding to the region. Since the entire input gradation region includes 256 gradations and the divisional number is 8 in this example, the gradation range in each of the regions is a region on every 32 gradations. Accordingly, the characteristic detection accuracy for the input video signals can be improved by making the divisional number larger and the number of gradation smaller in each of the divisional regions but, since improvement for the accuracy may also lead to increase of the circuits, the accuracy may be changed depending on the application use. the luminance distribution is detected by counting the number of data on every gradation region is in the first gradation region counter 29, the second gradation region counter 30 and the n_{th} gradation region counter 31 by the clock from the input video data gradation region detection section 28 and holding the same as the luminance distribution data by the first

distribution data latch circuit 32, the second distribution data hold latch 33 and the n_{th} distribution data hold latch 34 during the period set by the detection setting section 26.

For the detection of the average luminance value, the average luminance is detected on every 1 frame by multiplying each of the outputs from the first gradation region counter 29, the second gradation region counter 30 and the n_{th} gradation counter 31 by the m · multiplier circuit 35, the 2:m · multiplier circuit 36 and the n*m · multiplier circuit 37 respectively, adding each of the outputs by the adder circuit 38, dividing the output by the n*m · divider circuit 39 and holding the output for the period set by the detection setting section 29 (during 1 frame in this embodiment) as the average luminance data by the average luminance data · hold latch 40. m means the number of gradations in each of the divisional regions. As described above, since the input is set as 256 gradations and the number of division is set as 8, m is 32 in this embodiment. Accordingly, if each of the multiplier circuits 35 - 37 and the adder circuit 38 is constituted with 16 bits, the divider circuit 39 conducts division by: n*m = 8*32 = 256, which can be attained by a simple logic of rightward shifting by 8 bits (selection for higher 8 bits).

For the maximum · minimum value detection of the luminance, the input video data and the output from the dot data latch circuit 43 and the dot data latch circuit 44 each delayed by 1 clock thereto are inputted to the comparison circuit 41 and the comparison circuit 42, each of which judges the larger and the smaller data and outputs the same. That is, since the video data are sent serially, the output from dot data latch circuit 43 and the video data are compared in the comparison circuit 41 and larger data is always selected and outputted to the dot data latch circuit 43, and all video data for 1 frame are compared to obtain the maximum luminance data on every 1 frame. Further, the minimum luminance data can also be obtained in the same manner by the comparison circuit 42 and the dot data latch circuit 44. The output data are latched in the dot data latch circuit 43 and the dot data latch circuit 44 respectively and the outputted maximum and minimum luminance data are held for 1 frame by the maximum luminance data hold latch 45 and the minimum luminance data hold latch 46, respectively, during the period set by the detection setting section 26, to detect the maximum luminance and the minimum luminance on every 1 frame.

Then, details for the polygonal point generation sections 16 to 18 shown in Fig. 1 or 2 are to be explained with reference to Fig. 5.

Fig. 5 is a constitutional view for the inside of the polygonal point generation sections 16 - 18.

In Fig. 5, are shown an input image characteristic feed back control section 47 for reflecting the input characteristic detected by the input video image characteristic detection sections 13 - 15 by way of the microcomputer control section 24 upon setting the polygonal line point, a register write clock generation section 48 for polygonal line point setting register, and polygonal line point setting registers 49 - 57 holding polygonal line points respectively. While each of the polygonal point generation sections 16 - 18 includes three systems in Fig. 2, since all of the systems have the same constitution, description is to be made for 1 system in Fig. 5.

Further, in the description for Fig. 5, like that in the explanation for the input video image characteristic detection sections 13 - 15, an example of setting the number of input gradations to 256 gradations and dividing the entire input gradation region by 8 is to be explained. At first, the first characteristic example not reflecting the result of detection by the input video image characteristic detection sections 13 - 15 is to be explained. The first characteristic example is that of setting a characteristic equivalent between the input and the output irrespective of the result of the characteristic detection from the input

video image characteristic detection sections 13 - 15. The input video image characteristic feed back control section 47 directly sets each of the polygonal line point master data from the microcomputer control section 24. Accordingly, in the first characteristic example, linear characteristic data is directly set from the microcomputer control section 24. Fig. 6 shows the input/output gradation characteristic by this setting. In Fig. 6, the input/output equivalent (linear) characteristic is obtained by making the number of gradations between each of the divisional regions (the number of gradations for 1 divisional region = 256/8 = 32 gradation). Details for the operation of the input video image characteristic feed back control section 47 for setting linear characteristic is to be explained specifically with reference to Fig. 7.

Fig. 7 is a constitutional view of the input video image characteristic feed back control section 47. In Fig. 7, are shown a switching circuit 58 for switching the polygonal line point correction data and the polygonal line point · master data from the microcomputer control section 24, a polygonal line point correction data holding register 59, a polygonal line point data generation section 60 for generating the data from the polygonal line point correction data and the polygonal line point · master data, and a switching circuit 61 for selecting the output from the

switching circuit 58 or the polygonal line point data generation section 60 respectively. At first, for the first characteristic example for setting the linear characteristic shown in Fig. 6, the switching circuit 58 always selects (1) and the switching circuit 61 always selects (1). Accordingly, irrespective of the operation of the a polygonal line point correction data holding register 59 and the polygonal line point data generation section 60, the polygonal point · master data from the microcomputer data control section 24 is outputted directly as the set data for the polygonal line point register and set to the polygonal line point setting registers 49 - 57. The polygonal line point setting register 49 outputs polygonal line point 0, the polygonal line point setting register 50 outputs polygonal line point 1, the polygonal line point setting register 51 outputs the polygonal line point 2, the polygonal line setting register 52 outputs the polygonal line point 3, the polygonal line point setting register 53 outputs the polygonal line point 4, the polygonal line point setting register 54 outputs the polygonal line point 5, the polygonal line point setting register 55 outputs the polygonal line point 6, the polygonal line point setting register 56 outputs the polygonal line point 7 and the polygonal line point setting register 57 output the polygonal line point 8.

The first characteristic example of the linear input/output characteristic has been explained above and other examples of input/output characteristics will be explained below successively with reference to the drawings.

At first, as a second characteristic example, an example of setting the polygonal line point while reflecting the luminance distribution characteristic from the input video image characteristic detection sections 13 - 15 is to be explained. The second characteristic example is that of emphasizing a gradation region of high generation frequency by increasing the output luminance relative to the input gradation region of the highest generation frequency in the detected luminance distribution characteristic.

Fig. 8 shows an example of the input/output gradation characteristic set by the second characteristic example. In this example, the input video image characteristic detection sections 13 - 15 decides that the generation frequency of the input gradation data is highest in the divisional region 5 to emphasize the luminance characteristic in this region. That is, the microcomputer 23 determines the gradation region of the highest generation frequency based on the gradation data generation frequency detected by the luminance distribution detection section described with reference to Fig. 4. As a result, when the

frequency is highest for the region 5, a gradation value (a) is set to the polygonal line point correction register 59 of the input image characteristic feed back control section 47 shown in Fig. 7 and the gradation data obtained by addition of the master data at the polygonal line point 5 and the set value for the polygonal line correction register 59 is set to the polygonal line point 5 setting register 54 in the polygonal line point data generation section 60 by the control from the microcomputer 23. Since this makes the luminance characteristic in the region 5 further abrupt to increase the contrast in the gradation region 5, video images can be emphasized further.

Then, as a third characteristic example, explanation is to be made for an example of also setting the polygonal line point by reflecting the luminance distribution characteristic from the input video image characteristic detection sections 13 - 15. In this example, the input gradation region is divided into two groups of a lower region (region 1 - region 4) and a higher region (region 5 - 8) and controlled such that black color is emphasized where the region including greatest luminance distribution from the input video image characteristic detection sections 13 - 15 is in the lower region and, on the contrary, white color is emphasized where such region is in the higher region. In this case, the operation where the region including the

greatest luminance distribution is in the regions 5 - 8 is identical with the operation of the second characteristic example shown in Fig. 8, explanation therefor will be omitted. On the other hand, the operation where the region including the greatest luminance distribution is in the regions 1 - 4 is to be explained with reference to Fig. 9.

Fig. 9 shows an input/output gradation characteristic example by the third characteristic example. In this example, the input video image characteristic detection sections 13 - 15 decides that the generation frequency of the input gradation data is highest for the divisional region 4. That is, in the same manner as the operation for the second characteristic example, the region of the highest generation frequency is judged by the control of the microcomputer 23. Since this is the region 4 in this example, the microcomputer 23 sets the correction gradation value (b) to the polygonal line point correction register 59 of the input video image characteristic feed back control section 47 shown in Fig. 7, and sets the gradation data obtained by subtracting the set value at the polygonal line point correction register 59 from the master data of the polygonal line point 3 to the polygonal line point 3 setting register 52. In this case, the polygonal line point data generation section 60 constitutes a subtraction circuit. Since this makes the luminance characteristic in the region

4 further abrupt to increase the contrast of the region 4, the video images can be emphasized.

Then, as a fourth characteristic example, an example of combining the second and third characteristic examples is to be explained. Also in this case, the polygonal line point is set by reflecting the luminance distribution characteristic from the input video image characteristic detection sections 13 - 15. The luminance distribution characteristic detection sections 13 - 15 control the divisional gradation regions including the great distribution and next to the greatest distribution so as to emphasize the feature of the video data.

Fig. 10 shows an input/output gradation characteristic example by the fourth characteristic example. In this example, the generation frequency of the input gradation data is highest for the divisional region 6 and it is next to the highest for the divisional region 4 in the input video image characteristic detection sections 13 - 15. That is, it is controlled such that the feature of the divisional gradation regions including the greatest distribution and next to the greatest distribution is emphasized, by adding the first correction value (a) for the polygonal line point correction register 59 and the master data of the polygonal line point 6 by the polygonal line point data generation section 60 for the divisional region

6 since this is a group of high input gradation region, while by subtracting the second correction value (b) for the polygonal line point correction register 59 from the master data for the polygonal line point 3 by the polygonal line point data generation section 60 since this is a group of low input gradation region. In this case, the polygonal line point data generation section 60 constitutes both of the addition circuit and the subtraction circuit.

Then, as a fifth characteristic example, an example of setting the polygonal line point by reflecting the result for the detection of the maximum luminance value and the minimum luminance value from the input video image characteristic detection sections 13 - 15 is shown.

Fig. 11 shows an example of an input/output gradation characteristic reflecting the result of the maximum luminance detection. In this example, the dynamic range of the regions 1 to 7 is made largest when the maximum luminance is contained in the region of the divisional region 7 and not present in the divisional region 8. For this purpose, the set value for the polygonal line point 7 is made equal with the set value for the polygonal line point 8 for the polygonal line points 0 - 7, by the input video image characteristic feed back control section 47 in Fig. 5, and the intersection between the boundary of each of the signal regions and a line connecting the polygonal line point 0 and

the polygonal line point 7 is defined as each of set values from the polygonal line point 1 to the polygonal line point 6. This can provide the display characteristic of making the entire luminance characteristic uniform and expanding the high luminance area, by utmost utilizing the contrast of the display device.

In the same manner, Fig. 12 shows an example of an input/output luminance characteristic reflecting the result of detection for the minimum luminance. In this example, the dynamic range is made largest when the minimum luminance is contained in the region for the divisional region 1 and not contained in the divisional region 0. That is, the set value for the polygonal line point 1 is made equal with the set value for the polygonal line point 0 and the intersection between the boundary for each of the divisional regions and a line connecting the polygonal line point 1 and the polygonal line point 8 is defined as each of the set values from the polygonal line point 2 to the polygonal line point 7. This can provide the display characteristic of making the entire luminance characteristic uniform and expanding the low luminance area by utmost utilizing the contrast of the display device.

As described above, satisfactory display can be obtained by reflecting the result of detection from the input video image characteristic detection sections 13 - 15

to the luminance point generation sections 16 - 18 for the luminance characteristic provided to the video data, and various input/output gradation characteristics can be obtained. It will be apparent that the input gradation characteristic can be changed without reflecting the result of detection by the input video image characteristic detection sections 13 - 15.

Then, the inter-point gradation operation sections 19 - 21 in Fig. 2 are to be explained with reference to Fig. 13. The inter-point gradation operation sections 19 - 21 are used for converting the input gradation data into the inter-point output gradation data in accordance with the polygonal line points set by the polygonal point generation sections 16 - 18.

Fig. 13 shows a constitutional view of the inter-point gradation operation sections 19 - 21. Depending on the input form to the input video image characteristic detection sections 13 - 15 each of the inter-point gradation operation sections 19 - 21 has three systems when the data is inputted in the RGB form so as to set the data independently of each other, or has 1 system when the data is inputted in the form of the luminance data (Y) by the output from the luminance signal generation section 9 since processing is conducted in common with R, G and B. In Fig. 13, are shown a selector circuit 62 for selecting one of 8 set values other than the

uppermost gradation among the polygonal line point set values from the polygonal point generation sections 15 - 18, a selector circuit 63 for selecting one of 8 set values other than the lowermost gradation, among the polygonal line point set values and a gradation operation control section 64 for determining the inter-point gradation data from the polygonal line point set values selected by the selector circuit 62 and the selector circuit 63. In this illustrated example, the entire input gradation region is divided into 8 portions and the input image data include 256 gradations (8 bits) in the same manner as described above. Further, since the input video data are on the 8 bit base, this is indicated as IND [7:0]. Further, the polygonal points 0 - 8 are indicated, respectively, as POS0 - POS8.

At first, the polygonal line point set values are selected by the selector circuit 62 and the selector circuit 63 respectively by the higher 3 bits IND [7:5] in the input video data IND [7:0]. POS values are inputted to the selector 62 from the bottom in the order of register POS0 to POS7, while inputted to the selector 63 from the bottom in the order of registers POS1 to POS8. Accordingly, when the higher three bit IND [7:5] of the input image data are "000", the selector circuit 62 selects POS0 while the selector circuit 63 selects POS1. In the same manner, when IND [7:5] are "001", the selector circuit 62 selects POS1

while the selector circuit 63 selects POS2. Subsequently, POS0 - POS8 are selected in accordance with the value for IND [7:5] by the circuit 62 and 63 in the same manner. The set values selected by each of the selectors are inputted to the gradation operation control section 64 which conducts operation processing to obtain gradation data of the output video images. The gradation operation control section 64 conducts the operation, for example, in accordance with the following equation.

OUTD [7:0] = SEL1 + (SEL2 - SEL1) × IND [4:0]/32

OUTD [7:0] is the gradation data after operation outputted from the gradation operation control section 64, SEL1 represents a polygonal line point selected by the selector 62 and SEL2 represents a polygonal line point selected by the selector 63. Fig. 14 shows a gradation characteristic graph for explaining the equation described above, taking notice on one divisional region. Further, this shows a case when the higher 3 bit IND [7:5] of the input video data IND [7:0] are "100".

It can be seen that the selector 62 selects POS4 while the selector 63 selects POS5 in accordance with the operation of the inter-point gradation operation sections 19 - 21 and the input image data IND [7:0] are data in the region 5. Then, the gradation operation control section 64 calculates the output gradation OUTD [7:0] for lower 5 bit

IND [4:0] of the video data in accordance with the formula described above connecting POS4 and POS5 by a linear line and outputs them. The outputted OUTD [7:0] are obtained by conversion of the input video data IND [7:0] in accordance with the characteristic as shown in Fig. 6, Fig. 8 - Fig. 12, and OUTD [7:0] are outputted to the display panel 4 and displayed as picture images.

As described above, according to the first embodiment of this invention, the luminance characteristic can be set in accordance with the gradation distribution characteristic and the maximum luminance and the minimum luminance of the input video data on every frame period and, the video image can be displayed clearly, particularly, by emphasizing the contrast in the gradation distribution region of the highest gradation frequency and, further, it is possible to attain display while utmost utilizing the contrast characteristic of the display device in accordance with the maximum luminance and the minimum luminance.

In the first embodiment, the microcomputer 23 conducts processing so as to obtain a desired gradation characteristic based on the characteristic of the input video signals detected by the input video image characteristic detection sections 13 - 15 by using the microcomputer 23 and the microcomputer control section 24 and controls the polygonal point generation sections 16 -

18 and the inter-point gradation operation sections 19 - 21, to convert the gradation characteristic of the input video signals and output the same to the display panel. Then, for making the circuit structure simpler, the characteristic of the input video signals detected by the input video image characteristic detection sections 13 - 15 may be directly inputted to the polygonal point generation sections 16 - 18 without using the microcomputer 23 and the microcomputer control section 24. In this case, flexible control by the software of the microcomputer 23 is no more utilized and the control operation is fixed by the circuits but the number of parts relevant to the microcomputer 23 can be saved. Accordingly, the circuits of this embodiment can be incorporated in the liquid crystal module and it is possible to attain a liquid crystal module capable of optimally setting the gradation characteristic by itself in accordance with the video signals.

Fig. 15 is a constitutional view illustrating a second embodiment of using the technique according to this invention.

This embodiment additionally comprises a back light control section 65 for controlling the amount of a light of a back light in addition to the first embodiment. Since other portions are identical with those described for the first embodiment, detailed explanations are omitted.

Fig. 16 shows the concept control for the amount of a light of the back light. The light amount of the back light is controlled by the result of detection for the average luminance by the input video image characteristic detection sections 13-15. The average luminance is obtained by calculating the luminance value Y from the inputted video data and determining the average for the luminance value Y for 1 frame. In the second embodiment, the light amount of the back light is increased when the average luminance is high and the light amount of the back light is decreased when the average luminance is low. Then, in addition to the constitution of the first embodiment of displaying the input video date through gradation conversion on a liquid crystal display by controlling the amount of the back light in accordance with the average luminance, the apparent luminance can further be increased or decreased as shown in Fig. 16. This provides a feature of making brightness/darkness conspicuous on the video image display to display dynamic video images.

Fig. 17 shows an example of a flow chart for the back light controlling operation according to this embodiment. At first, polygonal line point set values are set to the polygonal point generation sections 16-18 by the microcomputer 23 and the microcomputer control section 24. The polygonal line points set in this case are as explained

for the first embodiment. Further, the average value for the luminance to the input image data is determined simultaneously by the input video image characteristic detection sections 13 - 15. The microcomputer 23 conducts processing along the flow chart shown in Fig. 17 in accordance with the average value for the luminance. At first, the microcomputer 23 confirms whether the average luminance value is higher than the gradation in the region 3 or not. If it is not higher than the region 3, the input image data is judged to be darker and the amount of the back light is decreased by the back light control section 65. For the extent of decreasing the light amount, it is assumed, for example, that the accuracy for the determined average luminance is 256 gradations (8 bit) and the light control range of the back light is also 256 steps (8 bit) and the point at which the control value for the back light agrees with the average luminance data is defined as a satisfactory display state. Since the input video image characteristic detection sections 13 - 15 update the detection data by the interval determined by the detection setting section 26, the back light is controlled again in accordance therewith. In this case, the data detecting interval is defined as 1 frame. If the average value for the detected luminance is higher than that of the region 3, it is then confirmed whether the value is lower than that of the region 6 or not. If it is

lower than that of the region 6, the detected average luminance is after all higher than the region 3 and lower than the region 6, so that the light amount of the back light by the back light control section 65 is not controlled. On the contrary, if it is judged not lower than that of the region 6, the input video data is judged to be brighter video images and the amount of the back light is increased by the same algorithm as in the darker video images. That is, since an appropriate amount of the back light can be obtained in accordance with the video data, video images can be displayed clearly.

As described above, the second embodiment of controlling the amount of light of the back light in accordance with the average luminance of the video signals has an effect capable of effectively utilizing light emitted from the back light. Since the liquid crystal does not emit light by itself but controls the amount of light transmitting the liquid crystal in accordance with the display data, a back light is necessary for the display. However, since the back light has always to emit light during display and, particularly, if the display content is a dark video image scene, most of the light from the back light is shielded by the liquid crystal, and it is not preferred in view of the efficiency for utilizing light. However, according to the second embodiment of this invention, since

the amount of light of the back light is increased or decreased in accordance with the average luminance, the amount of light of the back light is decreased for darker video images, while the amount of light of the back light is increased for brighter video images. Accordingly, the efficiency of utilizing the around of light of the back light can also be improved, or the electric power consummation for emitting the back light can also be reduced.

As described above, according to this invention, the gradation characteristic can be set in accordance with the gradation distribution characteristic and the maximum luminance and the minimum luminance of the input video data on every frame period and, particularly, by emphasizing the contrast of the gradation distribution region of the highest generation frequency, video images can be displayed clearly and, further, it is possible to conduct display while utmost utilizing the contrast characteristic of the display device in accordance with the maximum luminance and the minimum luminance.

Further, a liquid crystal module capable of optimally setting the gradation characteristic by itself in accordance with the input video signal can be attained by incorporating the circuits of this embodiment in the liquid crystal module.

Furthermore, by controlling the amount of light of the back light in accordance with the average luminance of video signals, the efficiency of utilizing the light of the back light can be increased and the electric consumption power for emitting the back light can be reduced.

Then, a third embodiment according to this invention is to be explained with reference to Fig. 18 through Fig. 24. The third embodiment is an example of a liquid crystal display device for conducting gradation correction in accordance with the video image characteristic described for the first embodiment, having a more concrete constitution of detecting the luminance distribution and conducting gradation correction in accordance therewith, and conducting the gradation correction without using the microcomputer control section 24.

At first, each of the drawings used for the explanation of the third embodiment is outlined and reference numerals depicted in each of them are explained.

Fig. 18 is a block diagram for the third embodiment of the liquid crystal display device applied with this invention, in which are shown a color video signal 71 sent from a signal source such as a personal computer or TV tuner, a histogram detection circuit 72 for detecting the distribution of the brightness in 1 frame of the color video signal 71, a histogram value 73 outputted from the histogram

detection circuit 72, a gradation control point calculation circuit 74 for calculating the gradation control point for γ-correction from the histogram value 73, a gradation control point 75 calculated by the gradation correction point calculation circuit 74, an arbitrary curve γ-correction circuit 76 for correcting the gradation of the color video signal 71 by an arbitrary curve from the gradation control point 75, color display data 77 put to gradation correction by the arbitrary curve γ-correction circuit 76 and a liquid crystal module 78 for color display with color display data 77.

Further, Fig. 19 is a view illustrating the constitution of the histogram detection circuit 72 in Fig. 18, in which are shown a Y value calculation circuit 79 for calculating the Y value representing the brightness from the color video signal 71 and a Y value 80 calculated by the Y value calculation circuit 79. There are shown a pulse generation circuit 81 and pulse signals 82, 83, 84, 85, 86, 87 and 88. The pulse generation circuit 81 generates one of plurality of pulse signals 82, 83, 84, 85, 86, 87 and 88 in accordance with the y value. Counters 89, 90, 91, 92, 93, 94 and 95 count up the plurality of pulse signals, respectively, and each of the outers is cleared on every 1 frame. The number of pulses on every frame can be counted up. 96, 97, 98, 99, 100, 101 and 102 each represents the

counted value counted up by the counter and 103 denotes a latch, which latches each of the counted value on every 1 frame and holds its temporarily. Each of 104, 105, 106, 107, 108, 109 and 110 denotes a latched counted value, which is the histogram value 73 described above.

Further, Fig. 20 is a view illustrating an example of the circuit for the Y value calculation circuit 79 in Fig. 19. When R video signal is shifted rightward by 2 bits, 0.25 R signal is outputted and when R video signal is shifted rightward by 4 bits, 0.0625 R signal is outputted. When 0.25 R signals and 0.625 R signals are added, 0.3125 R signal is outputted. When G video signal is shifted rightward by one bit, 0.5 R signal is outputted and when G video signal is shifted rightward by 4 bits, 0.0625 G signal is outputted. When 0.5 G signal and 0.0625 G signal are added, 0.5625 G signal is outputted. When B video signal is shifted rightward by 3 bits, 0.125 B signal is outputted. Then, when 0.3125 R signal, 0.5625 G signal and 0.125 B signal are added, a luminance signal (Y) is obtained.

Further, Fig. 21 is a view illustrating the constitution of the gradation control point calculation circuit 74 in Fig. 18, in which are shown a normalizing circuit 111 for normalizing the histogram value 73 for the brightness of the color video signal in 1 frame detected by the histogram detection circuit 72 to a constant average

value, a correction value calculation circuit 112 for calculating a correction value from the normalized histogram value, a correction intensity generation circuit 113 for generating a correction intensity k representing the intensity of correction, a reference characteristic generation circuit 114 for generating a gradation correction characteristic as the reference, and an adder 115, in which the output of the adder 115 forms the gradation control point 75. Further, Fig. 22 is a view illustrating the constitution of the arbitrary curve γ-correction circuit 76 in Fig. 18, in which each of polygonal line approximation circuits 116, 117 and 118 conducts gradation conversion of the color display data 71 constituted with RGB, which conducts gradation conversion and then outputs the color display data 77 constituted with RGB. Further, Fig. 22 shows details of a circuit only for the R color in the color video signals 71 constituted with RGB. Since circuits for G color and B color can be constituted in the identical manner, they are not illustrated. There are also shown selectors 119, 120 controlled by higher 3 bits of the R color video signals for selecting the correction coefficient 5, control points 121, 122 each selected by the selector 119, 120 and a linear approximation interpolation circuit 123 that conducts calculation by lower 5 bits of the R color video signal and control points 121, 122.

Further, Fig. 23 is a graph for the histogram value 73 outputted from the histogram detection circuit 72 in Fig. 18.

Further, Fig. 24 is a graph for the relation between the input gradation and output gradation of the arbitrary curve γ-correction circuit 76 in Fig. 18.

Then, operation of the third embodiment is to be explained specifically, in Fig. 18, the color video signal 71 is a color date representing RGB, which is color display data including video signals outputted from a personal computer and video signals of television broadcasting, as well as video signals regenerated from VTR and DVD, video images photographed by video cameras and video images prepared by computer graphics. The color video signal 71 is inputted to each of the histogram detection circuit 72 and the arbitrary γ-correction circuit 76. The histogram detection circuit 72 examines the frequency distribution of the brightness of the color video signals 71 in 1 frame and outputs the result as the histogram value 73 to the gradation control point calculation circuit 74. The gradation control point calculation circuit 74 calculates the gradation control point 75 for the correction of the gradation characteristic given to the arbitrary curve γ-correction circuit 76 based on the histogram value 73 and outputs the

same to the arbitrary curve γ-correction circuit 76. The arbitrary curve γ-correction circuit 76 conducts gradation correction on the color video signal 71 such that the relation between the input gradation and the output gradation forms a characteristic determined by the gradation control point 75 and outputs the result as the color display data 77 to the liquid crystal module 78.

Further, details for the operation of the histogram detection circuit 72 are to be explained with reference to Fig. 19, Fig. 20 and Fig. 23. Fig. 19 is a detailed constitutional view of the histogram detection circuit 72. The color video signal 71 inputted to the histogram detection circuit 72 is calculated for the Y value showing the brightness of the color video signal 71 in the Y value calculation circuit. In this embodiment, the color video signal 71 is RGB color signal and each of RGB comprises digital 8 bit data (256 gradation). Then, the Y value is defined as:

$$Y = 0.299R + 0.587G + 0.114B,$$

and the Y value is calculated from the RGB signals in accordance with the above mentioned equation. The Y value has a digital value of 8 bits.

By the way, referring to the practical calculation for the equation described above, an approximation calculation circuit as shown in Fig. 20 may be used for approximation

of the multiplication of a real number constant added to each of RGB values. Generally, the circuit scale of the multiplier is large and, particularly, since this is a real number multiplier, the scale is extremely increased. Then, the scale of the circuit can be reduced by the approximation for the calculation of the Y value, that is, approximation by bit shifting and addition instead of multiplication, while taking advantage that each of RGB has 8 bit digital value. In the approximation calculation circuit in Fig. 20, R color is calculated, for example, by adding the result of rightward shifting by 2 bits and rightward shifting by 4 bits to prepare 0.3125 R color signal. In the same manner, as shown in Fig. 20, 0.5625 G color and 0.125 B color are prepared by bit shifting and addition and finally adding all of them to determine the Y value 80. The thus obtained Y value 80 is then inputted to the pulse generation circuit 81.

The pulse generation circuit 81 is adapted to output one of pulse signals 82 to 88 in accordance with the Y value 80, and details of the operation are shown in Table 1.

TABLE 1

SECTION	Y VALUE 80	PULSE OUTPUT
1	0 ~ 31	PULSE SIGNAL 82
2	32 ~ 63	PULSE SIGNAL 83
3	64 ~ 95	PULSE SIGNAL 84
4	96 ~ 127	PULSE SIGNAL 85
5	128 ~ 169	PULSE SIGNAL 86
6	160 ~ 191	PULSE SIGNAL 87
7	192 ~ 223	PULSE SIGNAL 88
8	–	–

As shown in Table 1, pulse signal 82 is outputted when Y value 80 is 0 - 32, a pulse signal 83 is outputted when Y value 80 is 33-64, and in the same manner, pulse signals are outputted corresponding to the Y value 80. As described above, since the Y value 80 has a 8 bit digital value, its possible range is from 0 to 255. As will be described later in this embodiment, the range for the value of the Y value 80 is equally divided into 8 portions in accordance with the number of control points for conducting gradation correction of polygonal line approximation, and the value is divided on every 32 stages and the pulse is outputted in accordance with the Y value 80. In Table 1, there is no description for the portion corresponding to the section 8 in which Y value 80 shows values between 224 and 255. The circuit is not illustrated since the section 8 can be determined of itself when the section 1 - section 7 are determined exactly. That is, when the display resolution is, for example, 640 × 480 picture elements, since the total number of the picture elements is 307,200, it can be determined based on the total number of picture elements if the total number of pulses from section 1 to section 7 are known. As will be described later, the circuit corresponding to the section 8 is omitted since there is no

effect on the operation of this embodiment as will be described later.

As described above, the pulse generation circuit 81 outputs pulse signals 82 - 88 to the counters 89 - 95 respectively in accordance with the Y value 80. Each of the counters 89 - 95 counts up the pulses corresponding to section 1 - section 7 for the Y value 80. The value for each of the number of counted up pulses is temporarily held by a latch 103 on every 1 frame, which is outputted as the histogram value 73. Fig. 23 shows an example of the histogram value 73 as a graph. As shown in Fig. 23, the generation frequency of the Y value 80 is counted up on every sections to obtain the frequency distribution for the brightness of the color video signal in 1 frame.

Further, referring to histogram in Fig 23, the gradations of the sections H4, H5 and H6 of high frequency take a large portion in the color video signal 71 of the relevant frame and take a large area on the display screen when the color video signal 71 is displayed. On the other hand, the gradations of the sections H1 and H2 of low frequency have less ratio on the display screen. Accordingly, the display can be made conspicuous by emphasizing the contrast of the display data in the gradation section taking a large display area and suppressing the contrast of the display data in the

gradation section having less ratio in the display area. Then, the gradation characteristic may be determined directly from the frequency distribution of the histogram to convert the gradation characteristic of the display data.

Then, the operation of the circuit for calculating the gradation control point 75 from the histogram value 73 is to be explained with reference to Fig 21. Fig. 21 is a constitutional view for the gradation control point calculation circuit 74. The histogram value 73 obtained as described above is inputted to the normalizing circuit 111. The sum for the frequency for each of the histogram values 73 is equal with the display resolution and, for example, the sum of the frequency is 307,200 in a case of the resolution of 640 × 480 dots. Since the histogram value 73 is obtained as each frequency by equally dividing 0 - 255 that the Y value 80 can take into 8 portions, the simple average for the frequency in each of the sections is 38,400, that is, 1/8 for the sum of the frequencies. The normalization circuit 111 is a circuit for normalizing the value of 38400 of the simple average into 32. The frequency of each of the sections of the normalized histogram is expressed as normalized frequency H1 - H7 as shown in Fig. 21. Further, the simple average for the frequency after normalization is 32, which is expressed as δ.

Then, the normalized frequencies H1-H7 are inputted together with the correction intensity k from the correction intensity generation circuit 113 into the correction value calculation circuit 112 and the gradation correction values R1 - R7 for the gradation conversion are calculated. The correction value calculation circuit 112 is constituted with first to seventh correction value calculation circuits and each of the calculation circuits conducts the calculation in accordance with the following equations.

$$R_1 = K(H_1 - \delta)$$
$$R_2 = K(H_2 - \delta)+R_1$$
$$R_3 = K(H_3 - \delta)+R_3$$
$$R_4 = K(H_4 - \delta)+R_4$$
$$R_9 = K(H_6 - \delta)+R_6$$
$$R_7 = K(H_7 - \delta)+R_6$$

In the equations described above, the variant in each of them is as described in Fig. 21 and the equation means that the differences of the normalizing frequencies H1-H7 relative to the average δ of the frequency form the gradation correction values R1 - R7. Accordingly, when the value for the normalizing frequencies H1 - H7 is greater than the average δ, the gradation correction values R1 - R7 are positive and, when the value for the normalizing frequency

H1 - H7 is smaller than the average δ, the gradation correction value R1 - R7 are negative. Further, since the correction intensity k is added as a coefficient to each of the equations, the magnitude of the gradation correction values R1 - R7 can be changed by increasing or decreasing the value of the correction intensity k. With such calculation, the gradation correction values R1 - R7 are calculated and inputted to each of the adders 115.

The adder 115 is an addition calculator for correcting the reference points B1 - B7 of the gradation characteristic as s reference formed form the reference characteristic generation circuit 114 with the gradation correction values R1 - R7 calculated by the correction value calculation circuit 112 and the values after the addition form gradation control points L1 - L7. The reference points B1 - B7 for the gradation characteristics show the gradation characteristic as the reference for gradation correction of the color video signals 71, and a gradation characteristic is set to the reference in accordance with the histogram of the brightness.

The operation of the gradation control point calculation circuit 74 as described above is shown by concrete numerical values in Table 2.

TABLE 2

CONTROL POINT	NORMALIZATION FREQUENCE Hn	CORRECTION INTENSITY K	GRADATION CORRECTION VALUE Rn	REFERENCE POINT Bn	GRADATION CONTROL Ln
P_1	15		-8	32	24
P_2	32		-8	64	56
P_3	40		-4	96	92
P_4	48	0.5	4	128	132
P_5	49		12	160	172
P_6	38		15	192	207
P_7	18		8	224	232
	16				

AVERAGE VALUE OF NORMALIZATION FREQUENCY: $\delta = 32$ (CONSTANT)

Table 2 shows the operation of the gradation control point calculation circuit 74 for calculating the gradation from the histogram detected in 1 frame of the color video signal 71 numerical values. Example for the values of the frequencies H1-H8 of the normalized histograms are as shown in Table 2. The average value δ for the frequencies H1-H8 is 32. The correction value calculation circuit 112 conducts calculation for H1 - H7 among the normalizing frequencies H1 - H8 in accordance with the equation 2. That is, when the correction intensity k is 0.5, the gradation correction values R1 - R7 are calculated from each of the normalizing frequencies H1 - H7 as shown in Table 2. On the other hand, the reference points B1 - B7 show the characteristic as the reference for gradation conversion of the color video signal 71 and the gradation characteristic is corrected to the reference characteristic. The reference

points B1 - B7 in Table 2 have such values that the reference characteristic takes a linear characteristic. The gradation correction values R1 - R7 are added respectively to the reference points B1 - B7 to calculate the gradation control points L1-L7. The thus calculated gradation control points L1-L7 are outputted to the arbitrary curve γ -correction circuit 76.

Then, the operation of the arbitrary curve γ -correction circuit 76 for gradation correction of the inputted color video signal 71 by using the calculated gradation control points L1-L7 is explained with reference to Fig. 22. The arbitrary γ-correction circuit 76 comprises three polygonal line approximation circuits 116, 117 and 118 each of which conducts gradation conversion of the color video signal for each of RGB colors. In each of the polygonal line approximation circuits, the operation is explained here only for the R color circuit. Since the circuits for C color and B color conduct the same operation, explanations therefor are omitted. In Fig. 22, the R color video signal is 8 bit (256 gradation) video signal in which higher 3 bits are inputted as a selection control signal for the selectors 119 and 120. On the other hand, the lower 5 bits of the R color video signal is inputted to the linear approximation interpolation circuit 123, the data for the lower 5 bits of the R color video signal is expressed by

symbol c. The R color video signal of the higher 3 bits inputted to the selector 119, 120 selects the gradation control points L1 - L7 and a fixed value "0" F0 or a fixed value "255" F255 in accordance with the truth value table in Table 3.

TABLE 3

VIDEO IMAGE SIGNAL UPPER 3 BIT	SELECTOR 119 OUTPUT	SELECTOR 120 OUTPUT
000	FIXED VALUE "0"	L1
001	L1	L2
010	L2	L3
011	L3	L4
100	L4	L5
101	L5	L6
110	L6	L7
111	L7	FIXED VALUE "255"

The selected signals are inputted as control points 121 and 122 to the linear approximation interpolation circuit 123 respectively. The control point 121 is expressed as a and the control point 122 is expressed as b. Based on the thus selected control points a and b and the data c for the lower 5 bits of the R color video signal, the linear approximation interpolation circuit 123 outputs the R color gradation data after gradation correction calculated by the following equation:

$$y = a + (b-a) \cdot c/32$$

The inputted color video signal 71 is put to gradation conversion by the linear approximation interpolation circuit 123 defined by the equation described above and outputted as the color display data 77 to the liquid crystal module 78 and the images are displayed. As described above, the arbitrary curve γ-correction circuit 76 shown in Fig. 22 converts the color video signal 71 into arbitrary gradation characteristic by the input of the gradation control point 75 and outputs the same as the color display data 77 as shown in Fig. 22. Further, the gradation conversion characteristic is explained with reference to Fig. 24.

Fig. 24 shows an example of the γ-correction characteristic when the gradation conversion circuit according to this invention is applied to the reference characteristic of a linear characteristic. Description is to be made also with reference to Table 2. Since the reference characteristic is linear, each of the reference points B1 - B7 takes a value as shown in Table 2 and it is set such that the output gradation (reference point B1) is "32" for the input gradation "32" and the output gradation (reference) point B2) is "64" for the input gradation "gradation 64" and so on. According to the embodiment of this invention, the γ correction characteristic of polygonal line approximation is controlled by the control

points P1 - P7. The polygonal line approximation γ -characteristic obtained by increasing or decreasing the control points P1 - P7 in accordance with the gradation correction values R1 - R7 with respect to the reference points B1 - B7 constitutes the gradation conversion characteristic. In Table 2, gradation control points L1 - L7 are calculated by correcting the reference points B1 - B7 with the gradation correction values R1 - R7 and the gradation characteristic obtained by the gradation control points L1 - L7 form control points P1 - P7 in Fig. 24. After applying such gradation characteristic to the inputted color video signal 71 to conduct gradation conversion, they are outputted as the color display data 77 to the liquid crystal module 78.

As described above, according to the third embodiment, the display can be made conspicuous by emphasizing the contrast for the gradation of the section of higher frequency on the histogram and suppressing the contrast for the gradation of the section of lower frequency in accordance with the brightness histogram of the inputted color video signal 71. In addition, since the contract control is conducted corresponding to the color video signal, it can also cope with versatile video signals. Particularly, in video signals such as for dynamic images where video scenes change sequentially, since optimum

contrast control can always be applied, display can be conducted at an optimum image quality while considering the display characteristic and contrast of the liquid display device.

Then, a forth embodiment according to this invention is explained with reference to Fig. 18, Fig. 19, Fig. 25 to Fig. 28. In summary, the fourth embodiment has a feature capable of conducting gradation correction by changing the characteristics of the histogram detection circuit 72 in the third embodiment while taking the gradation characteristic inherent to the liquid crystal also into consideration. At first, explanation is to be made for each of the drawings and reference numerals depicted in each of them. Explanations for the reference numerals already explained for Fig. 18 and Fig. 19 are omitted.

Fig. 25 is a graph illustrating a relation between the amount of light transmitting the liquid crystal of the liquid crystal display device and electric signals (effective voltage value).

Fig. 26 is a graph illustrating a relation between the input display data (gradation data) to the liquid crystal display device to the liquid crystal display device and the light transmittance in the liquid crystal.

Fig. 27A and Fig. 27B are graphs showing the state of changing the section for each of the histogram distributions

relative to the relation between the input (gradation data) of the liquid crystal display device and the light transmittance in the liquid crystal.

Fig. 28 is a view showing a detailed constitution of the pulse generation circuit 81 in Fig. 19 for constituting the second embodiment, in which are shown a threshold value setting resistor 130, which is a circuit of generating threshold values S1 - S7 as a reference for comparison with the Y value 80 and a comparison circuits 131 - 137 for comparing the Y value 80 with the threshold values S1 - S7 to output pulses corresponding to the values determined in the threshold values S1 - S7.

Then, the operation of the fourth embodiment according to this invention is to be explained.

Fig. 25 shows a relation between the amount of light transmitting usual liquid crystal and a voltage applied to the liquid crystal (effective voltage value), in which the transmittance of the liquid crystal has an inverted S-shaped characteristic which saturates both at higher and lower transmittance areas. As described above, the liquid crystal has a nature of changing the transmittance of light and, in the liquid crystal display device, a light source (back light) is disposed at the back of the liquid crystal by utilizing this characteristic, the light from the back light is passed through the liquid crystal and the brightness is

changed by controlling the transmittance of the light in the crystal. Accordingly, the characteristic for the brightness of the liquid crystal display device is substantially equivalent with the characteristic shown in Fig. 25, providing that the transmittance of the liquid crystal on the ordinate is taken as the brightness of the liquid crystal display device in the characteristic chart. The display information for the display of the liquid crystal display device is given as the display data (gradation data). Most of the display data are those having a bit width capable of expressing multi gradations such as 6 bits (64 gradation) or 8 bits (256 gradation). Accordingly, for conducting display based on the display data, the liquid crystal display device incorporates a driver circuit for converting the display data into the liquid crystal application voltage. The driver circuit gives a relation between the display data (gradation data) and the transmittance of the liquid crystal as shown in Fig. 26. In most of liquid crystal devices, the inverted S-shaped liquid crystal transmittance characteristic is adjusted by the driver circuit such that the relation between the display data and the transmittance of the liquid crystal is substantially linear. However, the straight line sometimes include a curve portions due to scattering of the transmittance characteristic of the liquid crystal as shown

in Fig. 26. Then, for further correcting the transmittance characteristic of the liquid crystal, the histogram detection circuit 72 in Fig. 18 has a constitution as shown in Fig. 28.

In Fig. 28, a threshold setting register 130 outputs a plurality of threshold values S1 - S7 to comparison circuits 131-137 for comparison with the Y value 80. Further, the value for each of the threshold values S1 - S7 is freely set. The comparison circuits 131 - 137 compare the Y value 80 with the threshold values S1 - S7 and output pulse signals 82 - 88 in accordance with each of the results of comparison. The operation of the comparative circuits 131 - 137 is shown in Table 4.

TABLE 4

SECTION	Y VALUE 80		PULSE OUTPUT
1	0 ≦ VALUE < S1	0 ~ 39	PULSE SIGNAL 82
2	S1 ≦ VALUE < S2	40 ~ 72	PULSE SIGNAL 83
3	S2 ≦ VALUE < S3	73 ~ 101	PULSE SIGNAL 84
4	S3 ≦ VALUE < S4	102 ~ 128	PULSE SIGNAL 85
5	S4 ≦ VALUE < S5	129 ~ 155	PULSE SIGNAL 86
6	S5 ≦ VALUE < S6	156 ~ 184	PULSE SIGNAL 87
7	S6 ≦ VALUE < S7	185 ~ 218	PULSE SIGNAL 88

As shown in Table 4, the comparative circuit 131 outputs a pulse signal 82 when the Y value 80 is 0 or more and less than S1, the comparison circuit 132 outputs a pulse signal 83 when the Y value 80 is S1 or more and less than S2, the comparison circuit 133 outputs a pulse signal 84 when the Y value 80 is S2 or more and less than S3 and, in the same manner, each of the comparison circuits outputs a pulse signal in accordance with each of the threshold values. Accordingly, the threshold values S1 - S7 is a boundary value that defines each of the sections. Further, Table 4 also describes an example for the setting value of the threshold values S1 - S7. As shown by the example of the setting value in Table 4, the threshold values S1 - S7 for dividing the Y value 80 into 8 sections are arranged each at an uneven interval. This is, for correcting the gradation characteristic of the liquid crystal itself in which the slope to the gradation data is small at high and low transmittance areas and the slope is large at an intermediate transmittance area as shown in Fig. 26. Therefore, it is necessary to provide the gradation characteristic as shown in Fig. 27A, for which the threshold values S1 - S7 are set such that the width for the threshold value is wider for the sections with smaller Y value 80 and the width for the threshold value is narrower for the section with intermediate Y value 80. Therefore, the frequency is

relatively higher in the sections with smaller and larger Y value 80 relative to the section with the intermediate Y value 80. The γ-correction circuit of this invention serves to determine the gradation characteristic in accordance with the frequency in each of the sections of the histogram and emphasize the contrast of the section as the frequency is higher as has been described for the third embodiment. Accordingly, the γ-correction circuit operates so as to correct the gradation correction itself to the liquid crystal having the gradation characteristic shown in Fig. 26 and, as a result, a linear gradation characteristic can be provided for the liquid crystal display device.

Further, not only for adjusting the threshold values S1 - S7 to the gradation characteristic of the liquid crystal but also for making the entire gradation brighter as shown, for example, in Fig. 27 B, it is set to such a characteristic that the entire gradation characteristic is brighter relative to the linear characteristic. For this purpose, the threshold values S1 - S7 are set such that the width of the threshold value is wider in the section with a smaller Y value 80 and the width of the threshold value is gradually narrowed toward the section with larger Y value 80. In such an arrangement, the frequency is relatively higher in the section with smaller Y value 80 relative to the section

with larger Y value 80 and this functions to emphasize the contrast more in the gradation with smaller Y value 80, that is, the dark gradation. Accordingly, the gradation characteristic is set such that the entire gradation is brighter to obtain a liquid crystal display device of bright display.

As described above, according to the fourth embodiment of this invention, since gradation correction can be applied while taking the gradation characteristic inherent to the liquid crystal also into consideration by changing the setting for the threshold values S1 - S7 of the histogram detection circuit 72, it is possible to provide display of linear gradation characteristic as the liquid crystal display device. Further, it is possible to obtain a gradation characteristic capable of optionally setting the brightness as the liquid crystal display device.

Then, a fifth embodiment according to this invention is to be explained with reference to Fig. 29 and Fig. 30. The fifth embodiment is for moderating abrupt change of the gradation correction characteristic of the arbitrary curve γ-correction circuit 76 due to the change of the video image scenes in the dynamic image display in which the video image scenes change currently.

At first, each of the drawings is outlined and reference numerals depicted in each of them is to e

explained. Those portions carrying the same reference numerals as in the third and the fourth embodiments have already been explained and duplicate explanations therefor are omitted.

Fig. 29 is a block diagram of a liquid crystal display device applied with the fifth embodiment, in which are shown a low-pass filter 140 for moderating the change of the value to a gradation control point 75 and a gradation control point 141 moderated for the change, in which the gradation control point 141 is inputted for gradation correction to the arbitrary curve γ-correction circuit 76 also explained for the third and fourth embodiments.

Fig. 30 is a detailed constitutional view for the low-pass filter 140, in which are shown a digital filter 142, delay circuits 143, 144 and 145 for delaying the period by one frame respectively and an adder 146 under weighting. In Fig. 30, a digital filter to the gradation control point L1 is described. Since the constitution is identical also for digital filters for other gradation control points L2 - L7, their duplicated explanations are omitted.

Then, the operation of the fifth embodiment is to be explained.

In Fig. 30, an original gradation control point L1 inputted to the digital filter 142 is inputted to the delay circuit 143. Then, for the original gradation control point

L1, the delay circuit 143 outputs the gradation control point L1 delayed by 1 frame to the adder 146 and also to the delay circuit 144. Further, the delay circuit 144 outputs the gradation control point L1 delayed by 2 frames relative to the original gradation control point L1 to the adder 146 and also to the delay circuit 145. Further, the delay circuit 145 outputs the gradation control point L1 delayed by 3 frames to the original gradation control point L1 to the adder 146. Then, the adder 146 conducts addition under weighting for each of the delayed gradation control points L1. That is, all of them are added while weighting 1/2 to the original gradation control point L1, weighting 1/4 to the gradation control point L1 delayed by 1 frame and weighting 1/8 to each of the gradation control point L1 delayed by 2 frames and to the gradation control point L1 delayed by 3 frames, respectively. Concrete examples for numerical values are explained with reference to Table 5.

TABLE 5

FRAME	ORIGINAL GRADATION POINT	OUTPUT OF DELAY CIRCUIT 143	OUTPUT OF DELAY CIRCUIT 144	OUTPUT OF DELAY CIRCUIT 145	OUTPUT OF ADDER CIRCUIT 146
⋮	⋮	⋮	⋮	⋮	⋮
1	15	15	15	15	15
2	15	15	15	15	15
3	50	15	15	15	31
4	50	50	15	15	41
5	50	50	50	15	45
6	50	50	50	50	50
7	50	50	50	50	50
⋮	⋮	⋮	⋮	⋮	⋮

Table 5 shows the original gradation control point L1 and each of the delayed gradation control points and the values for the output from the adder 146 on every frames assuming a case that the value "15" of the gradation control point L1 up to first and second frames is abruptly changed to "50" at and after the third frame. As can be seen in Table 5, the output from each of the delay circuits 143, 144 and 145 is delayed each by one frame. Then, the delayed gradation control points are added each under weighting in the adder 146 and the output from the adder 146 takes values as shown in Table 5. As a result, abrupt change for the value of the original gradation control point from "15" to "50" between the second frame and the third frame is moderated as "15", "31", "41", "45", "50" from the second frame to the sixth frame. The value of the moderated gradation control point is outputted as a new gradation control point to the arbitrary curve γ-correction circuit 76.

As described above, abrupt change of the gradation correction curve along with change of the video image scenes can be moderated by the use of the low-pass filter 140 and, particularly, since the gradation correction curve also changes the characteristic gradually to currently changing video images such as of dynamic images, smooth video images can be displayed.

Then, a sixth embodiment of this invention is to be explained with reference to Fig. 31. The sixth embodiment is an example of a circuit for conducting gradation correction after storing the color video signal once in a frame memory and delaying the same by 1 frame.

Fig. 31 is a block diagram of a liquid crystal display device to which the sixth embodiment according to this invention is applied, in which are shown a frame memory 150 for delaying the color video signal 71 by 1 frame period and a color video signal 151 delayed by 1 frame. Since other portions are identical with those already explained for the third and fourth embodiments, duplicate explanations are to be omitted.

Then, the operation of the sixth embodiment is to be explained. In Fig. 31, inputted color video signal 71 is inputted to each of a histogram detection circuit 72 and a frame memory 150. The histogram detection circuit 72 detects the histogram showing the frequency of the brightness of the color video signal 71 to output a histogram value 73 as described for the first and second embodiments. Then, a gradation control point 75 is calculated based on the histogram value 73 by a gradation control point calculation circuit 74 to determine the gradation correction characteristic of an arbitrary curve γ -correction circuit 76. The histogram detection circuit 72

detects the histograms of the color video signal 71 of the frame successively and, after all of the color video signal 71 of the frame have been inputted for 1 frame, the detected histogram value 73 is latched and outputted. Accordingly, when the histogram value 73 is outputted, since the color video signal 71 of the frame next to the relevant frame is inputted, the histogram value 73 is delayed by 1 frame in view of the time relative to the color video signal 71. Accordingly, the gradation control point outputted from the gradation control point calculation circuit 74 is also delayed by 1 frame and determination for the gradation correction characteristic of the arbitrary curve γ-correction circuit 76 is also delayed by 1 frame.

In view of the above, the color video signal 71 is stored by using the frame memory 150 and then the color video signal 151 is outputted after delay for one frame period to the arbitrary curve γ-correction circuit 76. Both of the color video signal 151 and the gradation control point 75 inputted to the arbitrary curve γ-correction circuit 76 are delayed by 1 frame. Since the gradation control point 75 is calculated based on the color video signal 151 delayed by 1 frame, the gradation characteristic of the color video signal 151 of the relevant frame is aligned as it is in view of the time and reflected on the gradation control point 75,

which constitutes the gradation correction characteristic of the arbitrary curve γ-correction circuit 76.

As described above, in the sixth embodiment, since the frame memory for delaying the color video signal by 1 frame is provided, the gradation correction characteristic is determined based on the gradation characteristic of the color video signal of the relevant frame, so that gradation correction at higher accuracy can be applied to attain a liquid crystal display device of high image quality.

Then, a seventh embodiment according to this invention is to be explained with reference to Fig. 32. The seventh embodiment is an example of application not to the color video signal in which the color video signal 71 represents RGB but to a color video signal in which it is represented by Y/C signal (Y: brightness, C: color difference).

Fig. 32 is a block diagram of a liquid crystal display device to which the seventh embodiment according to this invention is applied and in which are shown a color difference signal 160 and a brightness signal 161, and the color video signal 71 comprises the color difference signal 160 and the brightness signal 161. 162 denotes a brightness signal undergoing gradation correction and 163 denotes a color decoder for converting the color difference signal 160 and the brightness signal 162 into RGB color signals. The

color decoder 163 is identical with a so-called RGB matrix circuit incorporated generally in television receivers for converting Y/C signals into RGB signals.

Then, the operation of the seventh embodiment is to be explained. The color difference signal 160 of the color video signal 71 is inputted to the color decoder 163. On the other hand, the brightness signal 161 is inputted to the histogram detection circuit 72 and the arbitrary curve γ-correction circuit 76. The histogram detection circuit 72 is identical with that shown in Fig. 19 in the same manner as for the third embodiment, but the Y value calculation circuit 79 in Fig. 19 not necessary since the inputted signal is already the brightness signal 161. Accordingly, the brightness signal 161 inputted to the histogram detection circuit 72 is directory inputted to the pulse generation circuit 81. The histogram detection circuit 72 detects the histogram showing the frequency of the brightness of the color video signal 71 and outputs the histogram value 73 as already described for Fig. 3 for the third and the fourth embodiments. Then, the gradation control point 75 is calculated based on the histogram value 73 in the gradation control point calculation circuit 74 to determine the gradation correction characteristic of the arbitrary curve γ-correction circuit 76. Then, the brightness signal 161 is corrected for the gradation characteristic by the

arbitrary curve γ-correction circuit 76. Then, the arbitrary curve γ-correction circuit 76 newly outputs the same as a brightness signal 162 to the color decoder 163. The arbitrary curve γ-correction circuit 76 is identical with that shown in Fig. 22 like that for the third embodiment but, since the inputted signal already consists only of the brightness signal 161, only one system may suffice for the polygonal line approximate circuit. The color decoder 163 converts the brightness signal 162 and the color difference signal 160 under gradation correction as described above into the RGB color display data 77. Then, the color display data 77 is inputted into the liquid crystal module 78 to display the images.

As described above, according to the seventh embodiment of this invention, gradation correction is applied in accordance with the histogram of the brightness of the relevant frame relative to the brightness signal and applies no correction at all to the color difference signal, so that change of hue or color spreading due to the gradation correction does not occur, and the gradation correction can be applied at high accuracy only for the brightness component to attain a liquid crystal display device of high image quality.

Then, an eighth embodiment according to this invention is to be explained with reference to Fig. 33. The

eighth embodiment is an example of a constitution incorporating a histogram detection circuit 72, a gradation control point calculation circuit 74, and an arbitrary curve γ-collection circuit 76 in a liquid crystal module.

At first, Fig. 33 is outlined and reference numerals therein are explained. Fig. 33 is a block diagram of a liquid crystal display device to which the eighth embodiment according to this invention is applied and in which are shown an interface circuit 171 comprising a histogram detection circuit 72, a gradation control point calculation circuit 74 and an arbitrary curve γ-correction circuit 76, a liquid crystal panel 172 in which picture elements are arranged in matrix, a data driver 173 for outputting a gradation driving voltage for the display of the liquid crystal panel 172 corresponding to the color display data 77, a scanning driver 174 for outputting a scanning voltage for the display of the liquid crystal panel 172, and a liquid crystal module 175 comprising the interface circuit 171, the liquid crystal panel 172, the data driver 173 and the scanning driver 174. Since other portions are identical with those already explained for the third embodiment, duplicate explanations are omitted.

Then, the operation of the eighth embodiment is to be explained. In Fig. 33, the interface circuit 171 applies gradation conversion to the color video signal 71 into the

color display data 77 and outputs the same to the data driver 173. The color video signal 71 inputted to the interface circuit 171 is inputted to the histogram detection circuit 72 and also to the arbitrary curve γ-correction circuit 76. The color video signal 71 inputted to the histogram detection circuit 72 which examines the frequency distribution of the brightness of the color video signal 71 in 1 frame and outputs the result as the histogram value 73 to the gradation control point calculation circuit 74. The gradation control point calculation circuit 74 calculates the gradation control point 75 for the gradation characteristic correction provided to the arbitrary curve γ-correction circuit 76 based on the histogram value 73 and outputs the same to the arbitrary curve γ-correction circuit 76. The arbitrary curve γ-correction circuit 76 applies gradation correction to the color video signal 71 such that the relation between the input gradation and the output gradation forms a characteristic determined by the gradation control point 75 and outputs the same as the color display data 77 to the data driver 173. The data driver 173 is a circuit for converting the inputted color display data 77 into the liquid crystal driving voltage and outputting the same to the liquid crystal panel 102 for display. On the other hand, the scanning driver 174 selects and scans the picture elements arranged in matrix on every rows and

applies a liquid crystal driving voltage outputted from the data driver 173 to each of the picture elements present in the row selected by the scanning driver 174 to conduct display on the liquid crystal panel 102. Since the operation of the interface circuit 171 is identical with that of the histogram detection circuit 72, the gradation control point calculation circuit 74 and the arbitrary curve γ-correction circuit 76 of the first embodiment, duplicate detailed explanations are omitted. It can make the display conspicuous on the liquid crystal panel 172 by emphasizing the contrast of the gradation for the section of higher frequency and suppressing the contrast of the gradation for the section of low frequency in accordance with the histogram corresponding to the histogram of the color video signal 71 inputted from the interface circuit 171. In addition, since the contrast control is conducted corresponding to the color video signal, it can also cope with various kinds of video signals. Particularly, since optimal contrast control can always be conducted also for the video signals such as of dynamic images in which video scenes change currently, display is possible at the optimum image quality while considering the display characteristic or the contrast of the liquid crystal panel 172. In addition, since the interface circuit 171 is incorporated together with the liquid crystal panel 172, the data driver

173 and the scanning driver 174 in the liquid crystal module 175, the liquid crystal module, particularly, optimal to the display of the dynamic images can be constituted in a compacted manner.

The first to eighth embodiments described above can be practiced also in combination of each of them.

For example, the fifth and sixth embodiments can be combined by inserting the low-pass filter 140 of Fig. 29 between the gradation control point calculation circuit 74 and the arbitrary curve γ-correction circuit 76 in the circuit shown in Fig. 31. In this embodiment, since the frame memory of delaying the color video signal by 1 frame is disposed, the gradation correction characteristic is determined based on the gradation characteristic of the color video signal in the frame, so that gradation correction at higher accuracy can be conducted, as well as provision of the low-pass filter can moderate the abrupt change of the gradation correction curve along with the change of the video image scenes and, particularly, since the gradation correction curve also change the characteristic gradually relative to the currently changing video images such as of dynamic images, smooth video images can be displayed and a liquid crystal display device of high picture quality can be attained.

Further, in the seventh embodiment, the inputted color video signal 71 is the Y/C signal. As a modified embodiment, the inputted color video signal 71 may be RGB signal and a color encoder for converting the inputted RGB signal once into the Y/C signal may be disposed and the Y/C signal outputted from the color encoder may be formed as the color video signal 71 in Fig. 32. In this modification of the seventh embodiment, since the gradation correction is conducted in accordance with the brightness histogram in the frame to the brightness signal and no correction is applied to the color difference signal, change of hue or color spreading does not occur and the gradation correction can be conducted at high accuracy only for the brightness component to attain a liquid crystal display device of high image quality.

Further, the interface circuit 101 of the eighth embodiment may be replaced with the circuit according to the fourth to seventh embodiments in addition to constituting the same with the circuit shown in Fig. 18 for the third embodiment. In this case, since the interface circuit 171 is incorporated together with the liquid crystal panel, the data driver and the scanning driver in the liquid crystal module, a liquid crystal module particularly optimal to the display of dynamic images can be constituted in a compact manner.

As described above, the embodiments according to this invention operates so as to emphasize the contrast of the gradation in the section of high frequency and suppress the contrast of the gradation in the section of low frequency in view of the histogram corresponding to the brightness histogram of the inputted color video signal, the display can be made conspicuous, as well as since the contrast control is conducted corresponding to the color video signal, it can cope with versatile video signals. Particularly, since optimal contrast control can always be conducted also for video signals such as for dynamic images in which video image scenes change currently, display can be conducted at optimal image quality in view of the display characteristic and the contrast of the liquid crystal display device and a liquid crystal display device of high image quality can be attained.

In addition, since the gradation correction also in view of the gradation characteristic inherent to the liquid crystal can be conducted by making the setting for the threshold value of the histogram detection circuit variable, it is possible to provide display of the linear gradation characteristic as the liquid crystal display device. Further, it is possible to obtain the gradation characteristic capable of freely setting the brightness as

the liquid crystal display device by the setting of the threshold value.

The present invention is not limited to the above embodiments and various changes and modifications can be made within the spirit and scope of the present invention. Therefore, to appraise the public of the scope of the present invention, the following claims are made.